

S/N 10/634174



PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Leonard Forbes	Examiner:	Tan N. Tran
Serial No.:	10/634174	Group Art Unit:	2826
Filed:	August 05, 2003	Docket:	1303.102US1
Title:	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME		

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**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No :10/634174

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The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

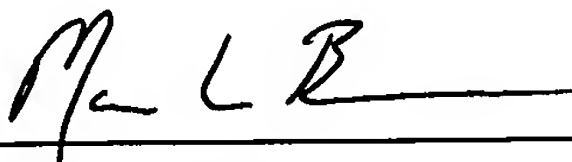
Respectfully submitted,

LEONARD FORBES

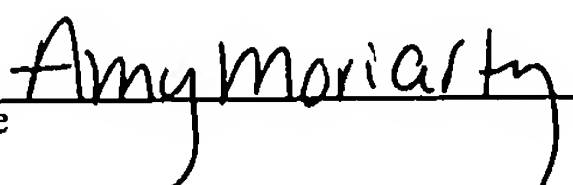
By his Representatives,

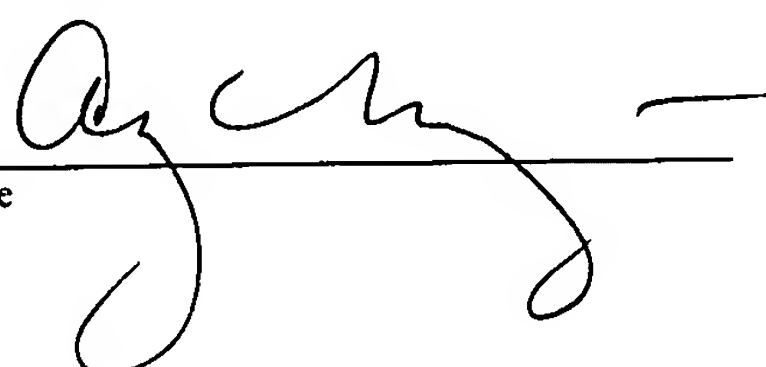
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(612) 373-6960

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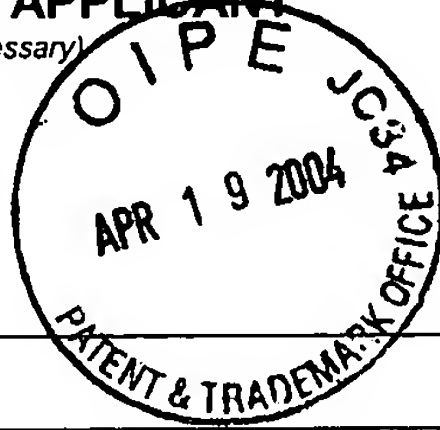
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 15th day of April, 2004.

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Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)	Complete if Known	
	Application Number	10/634174
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	First Named Inventor	Forbes, Leonard
	Group Art Unit	2826
	Examiner Name	Tran, Tan
Sheet 1 of 7	Attorney Docket No: 1303.102US1	



US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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	US20020070421	06/13/2002	Ashburn, Stanton P.	257	510	02/08/2002
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Substitute Disclosure Statement Form (PTO-1449)

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Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)	Complete if Known	
	Application Number	10/634174
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	First Named Inventor	Forbes, Leonard
	Group Art Unit	2826
	Examiner Name	Tran, Tan
Sheet 2 of 7	Attorney Docket No: 1303.102US1	

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Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
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Substitute Disclosure Statement Form (PTO-1449)

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Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
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Sheet 5 of 7	Attorney Docket No: 1303.102US1	

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<b>Examiner Name</b>	Tran, Tan

Sheet 6 of 7

Attorney Docket No: 1303.102US1

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**EXAMINER****DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

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Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b> (Use as many sheets as necessary)	Complete if Known	
	Application Number	10/634174
	Filing Date	August 5, 2003
	First Named Inventor	Forbes, Leonard
	Group Art Unit	2826
	Examiner Name	Tran, Tan
Sheet 7 of 7	Attorney Docket No: 1303.102US1	

		WIJARANAKULA, W. , et al., "Effect of preanneal heat treatment on oxygen precipitation in epitaxial silicon", <u>Materials Issues in Silicon Integrated Circuit Processing Symposium</u> , (April 1986),139-44	
		WIJARANAKULA, W. , et al., "Internal Gettering Heat Treatments and Oxygen Precipitation in Epitaxial Silicon Wafers", <u>Journal of Materials Research</u> , 1(5), Dept of Electr & Comput. Eng, Oregon State Univ., Corvallis, OR,(September-October 1986),693-7	
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SN 10/634174

PATENTIN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes

Examiner: Tan N. Tran

Serial No.: 10/634174

Group Art Unit: 2826

Filed: August 5, 2003

Docket: 1303.102US1

Title: STRAINED SI/SIGE/SOI ISLANDS AND PROCESSES OF MAKING SAME

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COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/379749	March 5, 2003	1303.089US1	MICRO-MECHANICALLY STRAINED SEMICONDUCTOR FILM
10/425797	April 29, 2003	1303.093US1	LOCALIZED STRAINED SEMICONDUCTOR ON INSULATOR
10/431134	May 7, 2003	1303.094US1	STRAINED Si/SiGe STRUCTURES BY ION IMPLANTATION
10/425484	April 29, 2003	1303.095US1	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
10/443340	May 21, 2003	1303.099US1	ULTRA-THIN SEMICONDUCTORS BONDED ON GLASS SUBSTRATES
10/431137	May 7, 2003	1303.100US1	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING
10/443337	May 21, 2003	1303.103US1	GETTERING OF SILICON ON INSULATOR USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/634174

Filing Date: August 5, 2003

Title: STRAINED SI/SIGE/SOI ISLANDS AND PROCESSES OF MAKING SAME

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Dkt: 1303.102US1

10/443339	May 21, 2003	1303.104US1	WAFER GETTERING USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
10/623794	July 21, 2003	1303.108US1	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
10/623788	July 21, 2003	1303.109US1	STRAINED SEMICONDUCTOR BY FULL WAFER BONDING
10/164611	June 10, 2002	Unknown	OUTPUT PREDICTION LOGIC CIRCUITS WITH ULTRA-THIN VERTICAL TRANSISTORS AND METHODS OF FORMATION

Respectfully submitted,

LEONARD FORBES

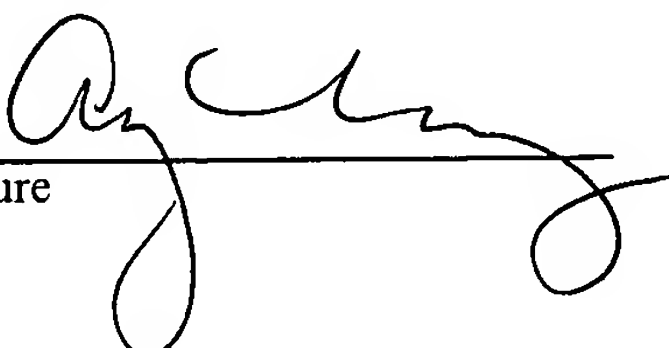
By Applicant's Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
P.O. Box 2938  
Minneapolis, MN 55402  
(612) 373-6960

Date 4-15-04 By   
Marvin L. Beekman  
Reg. No. 38,377

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